## REMARKS

The application includes claims 2-5, 7-9, 11-19, and 22-49 prior to entering this amendment.

The examiner rejects claims 2-5, 7-9, 11-19, and 22-49 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

The examiner rejects claims 44-46 and 49 under 35 U.S.C. § 102(e) as being anticipated by Grisamore (U.S. Patent No. 6,535,901).

The examiner rejects claims 2-5, 7-9, 11-12, 17-19, 22-27, and 47-48 under 35 U.S.C. § 103(a) as being obvious over Grisamore in view of Chang, et al. ("Hardware-Efficient Implementations for Discrete Function Transforms Using LUT-Based FGPAs").

The examiner rejects claims 13-16, and 28-31 under 35 U.S.C. § 103(a) as being obvious over Grisamore in view of Chang and Fang, et al. ("A Hierarchical Functional Structuring and Partitioning Approach for Multiple-FPGA Implementations").

The examiner rejects claims 32, 36-38, and 42-43 under 35 U.S.C. § 103(a) as being obvious over Grisamore in view of Greenberger (U.S. Patent No. 6,411,979).

The examiner rejects claims 33-35 under 35 U.S.C. § 103(a) as being obvious over Grisamore in view of Greenberger and Chang.

The examiner rejects claims 39-41 under 35 U.S.C. § 103(a) as being obvious over Grisamore in view of Greenberger, Chang, and Fang.

The applicants cancel claims 2-5, 7-9, 11-19, and 22-49 without prejudice.

The applicants add new claims 50-99.

The application remains with claims 50-99 after entering this amendment.

The applicants add no new matter and request reconsideration in view of the following remarks.

The applicants point out that the claimed subject matter may be patentably distinguished from the cited reference(s) for multiple reasons; however, the following remarks are believed to be sufficient. Likewise, the applicants note that their failure to comment directly upon any of the positions asserted by the examiner in the office action does not indicate agreement or acquiescence with those asserted positions.

## Claim Rejections - 35 U.S.C. § 101

The examiner rejects claims 2-5, 7-9, 11-19, and 22-49 because the claimed invention is directed to non-statutory subject matter. The applicants have obviated this objection by canceling these claims. The applicants believe that the new claims are directed to statutory subject matter.

## Claim Rejections - 35 U.S.C. § 102

The examiner rejects claims 44-46 and 49 as being anticipated by Grisamore.

The applicants address the applicability of Grisamore to new independent claims 50, 70, 85, and 93 and to selected ones of the dependent claims having related elements. The applicants believe that similar arguments are applicable to canceled independent claim 44.

Claim 50 recites:

*where the hybrid summing module is configured to receive as inputs the plurality of partial products, and is configured to reduce the plurality of partial products to a first partial summation and a second partial summation via the one or more full adders and the one or more half adders;*

*where outputs of each of the one or more full adders and outputs of each of the one or more half adders are coupled to inputs of respective ones of the plurality of registers; and*

*where any bits of the plurality of partial products that are not coupled to an input of one of the one or more full adders or to an input of one of the one or more half adders are coupled to inputs of respective ones of the plurality of registers.*

Claim 55 recites:

*The system of claim 50,*

*further comprising a summing module generator adapted to configure the hybrid summing module to reduce the plurality of partial products; and*

*where the combinational stage, the hybrid summing module, and the summing module generator are parts of a single integrated circuit.*

The examiner indicates that Grisamore teaches "wherein the elements comprise one or more adders having one or more associated registers and one or more additional registers (e.g. col. 1 lines 32-42 wherein appropriate registers at optimal points in each adder for pipelining and

col. 1 lines 36-38)"[1]. The examiner clarifies this interpretation in parts (a) and (d) of the Response to Arguments section of the most recent office action.[2]

Respectfully, the examiner is misinterpreting Grisamore's Figure 5, and is projecting into Grisamore the applicants' disclosure. Grisamore's Figure 5 "illustrates the operation of the reduction tree module 14."[3] The lines in Figure 5 separate columns of the reduction process; the groupings of dots represent full adders and half adders; and the arrows represent outputs from one full adder or half adder to another. There is no mention in Grisamore of registers associated with Figure 5. There is nothing in the teachings of Grisamore to enable one to construe the lines, the half adders, the full adders, or the arrows of Figure 5 as representing the recited registers. Although Grisamore indicates that an array multiplier "architecture provides the advantages of efficiency in integrated circuit layout and ease of pipelining by using registers at optimal points in the array multiplier,"[4] Grisamore does not disclose or identify the optimal points in the array multiplier and thus cannot serve as the basis for the examiner's rejection. Grisamore provides no basis to construe any specific placement of registers in the reduction tree module, let alone the applicants' specific placement of registers in the hybrid summing module as recited in claim 50 (with similar elements in claims 70, 85, and 96). Accordingly these claims (and their dependent claims) are in condition for the examiner's allowance.

Respectfully, the examiner is also misinterpreting the applicants' recited *summing module generator*. The examiner indicates Grisamore discloses "a summing module generator (e.g. part 14, 16, and 18 in Figure 1)."[5] But Grisamore's Figure 1 shows a fast multiple accumulator, and the cited parts 14, 16, and 18 are portions of the fast multiple accumulator. The fast multiple accumulator cannot disclose a summing module *generator*. In one embodiment, the summing module generator is invoked "to dynamically reallocate CLB atomic resources to generate and implement the hyperpipelined hybrid summing module architecture during execution of the logic device 200."[6] That is, in some embodiments, the summing module *generator* is used, at least in part, to generate (or configure or implement) the summing module as required by the claims. Grisamore does not disclose the summing module generator, as

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[1] Office Action, pages 3-4.
[2] Office Action, pages 15-18.
[3] Grisamore, col. 4, lines 44-45.
[4] Grisamore, col. 1, lines 36-38.
[5] Office Action, page 3.
[6] Application, page 9, lines 1-3.

recited in the applicants' claims 55, 70, 86, and 93. Furthermore, the applicants' summing module generator is recited as being part of an integrated circuit along with the hybrid summing module. As recited in the applicants' claim 55 (with similar elements in claims 70, 86, and 93): "where the combinational stage, the hybrid summing module, and the summing module generator are parts of a single integrated circuit." Even if one construes Grisamore's algorithm for generating a fast multiple accumulator as disclosing the applicants' summing module generator (an incorrect construction since the structures generated are different), there is no teaching in Grisamore of incorporating any of Grisamore's algorithms (as opposed to the logic produced by those algorithms) into an integrated circuit. Accordingly these claims (and their dependent claims) are in condition for the examiner's allowance.

As dependent claims 51-69, 71-84, 86-92, and 94-99 incorporate all of the elements of their respective independent claim, and as the independent claims are allowable for the reasons explained above, the dependent claims are also allowable.

**Claim Rejections - 35 U.S.C. § 103**

The examiner rejects claims 2-5, 7-9, 11-12, 17-19, 22-27, and 47-48 as being obvious over Grisamore in view of Chang. The examiner rejects claims 13-16, and 28-31 as being obvious over Grisamore in view of Chang and Fang. The examiner rejects claims 32, 36-38, and 42-43 as being obvious over Grisamore in view of Greenberger. The examiner rejects claims 33-35 as being obvious over Grisamore in view of Greenberger and Chang. The examiner rejects claims 39-41 as being obvious over Grisamore in view of Greenberger, Chang, and Fang.

The applicants address the applicability of Chang, Greenberger, and Fang to new independent claims 50, 70, 85, and 93 and to selected ones of the dependent claims having related elements. The applicants believe that similar arguments are applicable to canceled independent claims 2, 17, and 32.

The applicants' believe that all of claims 50-99 are allowable over the combination of Grisamore, Chang, Greenberger, and Fang. As explained above with regard to the 102 rejection, Grisamore does not teach the applicants' summing module generator, or the applicants' specific placement of registers in the hybrid summing module, and all of the applicants' claims incorporate one or both of these elements.

The 103 rejections rely on Chang disclosing ""the dedicated logic module"[7] (e.g., an FPGA). The applicants, however, have not relied on this element to distinguish any of the new independent claims.

The 103 rejections rely on Greenberger disclosing "in Figure 2 a complex arithmetic operation comprising two paths (e.g. real and imaginary wherein label with Zr and Zi) one for a real-component branch (e.g. left side of Figure 2) inverting certain partial products (e.g. 34.1 for subtraction) and passing the inverted and non-inverted partial products and one for an imaginary-component branch (e.g. right side of Figure 2), passing the partial products (e.g. 34.2 for addition)."[8] The applicants have not relied on this element to distinguish any of the new independent claims.

The 103 rejections rely on Fang disclosing "in Figure 3 a controller or a logic control module dynamically (e.g. left column 3rd paragraph page 1189 and Module1(DP) in Figure 3 and Figure 1) structures the atomic elements of the dedicated logic device (e.g. Figure 3)."[9] The applicants observe that Fang discloses "structuring" and "partitioning" of an FPGA. Fang does not, however, disclose the applicants' summing module generator, nor is Fang's "structuring" or "partitioning" performed by a portion of an integrated circuit that is itself an object of the "structuring" or "partitioning." As recited in the applicants' claim 55 (with similar elements in claims 70, 86, and 93): "where the combinational stage, the hybrid summing module, and the summing module generator are parts of a single integrated circuit." Further, as Fang does not disclose a structure for a hybrid summing module, and as all of the claims incorporate one or the other of these elements, all of the claims are allowable over Fang.

Accordingly, all of claims 50-99 are in condition for the examiner's allowance.

**Prior Art Made of Record**

The examiner indicates that U.S. Patent No. 7,007,059 to Mohammed, et al. is made of record. The applicants point out that the filing date of Mohammed (Jul. 30, 2001) is subsequent to the applicants' filing date (Mar. 31, 2001), and that, as far as the applicants can discern from public PAIR, Mohammed does not claim priority to any earlier filings.

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[7] Office Action, page 6.
[8] Office Action, page 12.

## Conclusion

For the foregoing reasons, the applicants request reconsideration and allowance of the remaining claims. The applicants encourage the examiner to telephone the undersigned at (503) 224-2170 if it appears that an interview would be helpful in advancing the case.

**Customer No. 73552**

Respectfully submitted,

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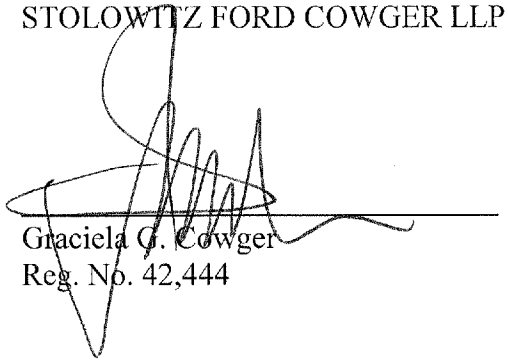

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[9] Office Action, page 10.